SYNCHRONIZER APPARATUS FOR SYNCHRONIZING DATA FROM ONE CLOCK DOMAIN TO ANOTHER CLOCK DOMAIN

ABSTRACT

[0030] An improved signal synchronizing circuit for prohibiting signals traveling from a first clock domain operating with a first clock to a second clock domain operating with a second clock when the first clock is not active. The synchronizing circuit comprising at least one signal receiving module for receiving at least one selected signal in the first clock domain, a detection circuit producing a detection signal indicating that the first clock is active, and at least one output selection module for passing the selected signal from the first clock domain to the second clock domain when the first clock is active.